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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,973	03/22/2001	Hideyuki Toriyama	245402002600	6050

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EXAMINER	
NGUYEN, MADELEINE ANH VINH	

ART UNIT	PAPER NUMBER
2626	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,973	TORIYAMA, HIDEYUKI	
	Examiner	Art Unit	
	Madeleine AV Nguyen	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This communication is responsive to amendment filed on February 24, 2005.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2, 3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 2 and 3 claims a second processing means for determining a characteristic of an image region (21, Fig.1) and a switch device (Fig. 2 or 4 or 6) while both of the region discriminating unit 21 and the switch are not included in one figure. If Fig.1 is the claimed invention of claim 2 or 3, there is no switch in Fig.1 and in Fig.2 or 4 or 6, there is no region discriminating unit 21. If the region discriminating unit 21 and the switch device are the claimed invention, they should be in one figure since in Fig.2 or 4 or 6 there is no region discriminating unit 21 as the second processing means.

3. The rejection of claims 1-28 is modified in light of Applicant remarks of the previous 112 rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-28 are rejected under 35 U.S.C. 102(e) as being anticipated byYoshida et al (US Patent No. 6,538,769).

Concerning claim 1, Yoshida discloses an image processing apparatus (Fig.2) comprising a first processing means (114, 125) for sequentially processing input pixel data; a memory device (126, 127, 135) provided at a preceding stage of the first processing means to store the pixel data; a second processing means (144, 131, 132, 133, 142) for determining characteristic of an image region including a plurality of the pixel data; a third processing means (136) for processing the pixel data processed at the first processing means, based on the characteristic determined by the second processing means (col. 4, lines 1 – col. 5, line 52).

Concerning claim 2, Yoshida discloses an image processing apparatus (Fig.2) comprising a first processing means (114, 125) for sequentially processing input pixel data; a second processing means (144, 131, 132, 133, 142) for determining characteristic of an image region including a plurality of the pixel data; a third processing means (136) for processing the pixel data processed at the first processing means, based on the characteristic determined by the second processing means; a connecting means

(connecting lines) for connecting a memory device (126, 127, 135); a switch device (112, 113, 134) for switching a circuit such that the connecting means (at switch 112 or 113) is arranged either at a preceding stage of the first processing means or (at switch 134) between the first processing means and the third processing means (col. 4, lines 1 – col. 5, line 52).

Concerning claim 3, Yoshida discloses an image processing apparatus (Fig.2) comprising a first processing means (114, 125, 140) for converting a plurality of color data into a plurality of image color data in a first state (125), and the plurality of color data into a plurality of image color data in a second state (114 or 140); a second processing means (144, 131, 132, 133, 142) for determining characteristic of an image region including a plurality of the pixel data; a third processing means (136) for processing the pixel data processed at the first processing means, based on the characteristic determined by the second processing means; a connecting means (connecting lines) for connecting a memory device (126, 127, 135); a switch device (112, 113, 134) for switching a circuit such that the connecting means (at switch 112 or 113) is arranged either at a preceding stage of the first processing means or (at switch 134) between the first processing means and the third processing means (col. 4, lines 1 – col. 5, line 52).

Concerning claim 4, Yoshida discloses an image processing apparatus (Fig.2) comprising a memory device (126, 127, 135); a first processing means (114, 125, 140) for sequentially convert and output the image data; a second processing means (144, 131, 132, 133, 142) for receive the same image data (Cb, Cr, V) as input into the memory device and to output data processed based on the received image data; a third processing

means (136) to receive the image data output from the first processing unit and the data output from the second processing unit, and to process the image data output from the first processing unit based on the data output from the second processing unit (col. 4, lines 1 – col. 5, line 52).

Concerning claims 5-12, Yoshida further teaches that the same image data (Cb, Cr, V) is input into the memory device and the second processing unit in parallel (Fig.2), (claim 5); the second processing unit (144) determines an attribute of an image region based on image data of a pixel to be processed and pixels on the periphery of the pixel to be processed, and outputs data indicating the attribute (col. 5, lines 38-45), (claim 6); the second processing unit determines if the image region is represented by a character or a photograph or a dot (col. 5, lines 38-45), (claim 7); the first processing unit converts the input image data into image data of a different color system (scanner 32) to output the converted image data, (claim 10); the third processing unit (136) processes the image data output from the first processing unit to correct sharpness of an image (col. 5, lines 47-50), (claim 11); the third processing unit (136) substantially simultaneously receives the image data from the first processing unit (114, 125, 140) and data corresponding to the image data from the second processing unit (144, 142, 131, 132, 133), (claim 12).

Concerning claim 13, Yoshida discloses an image processing apparatus (Fig.2) comprising a memory device (114, 124, 126, 135); a first processing means (114, 125, 140) for converting and output image data; a second processing means (144, 131, 132, 133, 142) to receive a plurality of the pixel data and to output data processed based on the input image data; a third processing means (136) to process image data output from the memory device (114, 124, 126, 127 or 135) and to output data processed based on the

input image data; a first circuit to input the image data output from the memory device (114, 124) into the first processing unit (114, 125); a second circuit to input the image data output from the first processing unit (114, 125) into the memory device (126, 127) and also to input the image data output from the memory device (126, 127) into the second processing unit (128-133, 143, 144); a switch device (112, 113, 134) for selectively switch the first and second circuit (col. 4, lines 1 – col. 5, line 52).

Concerning claims 14-19, Yoshida further teaches that the same image data (Cb, Cr, V) is input into the memory device and the second processing unit in parallel when the first circuit is selected by the switching device (Fig.2), (claim 14); the same image data is input into the first processing unit and the second processing unit in parallel when the second circuit is selected by the switching device (Fig.2), (claim 15); the second processing unit (144) determines an attribute of an image region based on image data of a pixel to be processed and pixels on the periphery of the pixel to be processed, and outputs data indicating the attribute (col. 5, lines 38-45), (claim 16); the first processing unit converts the input image data into image data of a different color system (scanner 32) to output the converted image data, (claim 17); the third processing unit (136) processes the image data output from the first processing unit to correct sharpness of an image (col. 5, lines 47-50), (claim 18); the third processing unit (136) substantially simultaneously receives the image data from the first processing unit (114, 125, 140) and data corresponding to the image data from the second processing unit (144, 142, 131, 132, 133), (claim 19).

Concerning claim 20, Yoshida discloses an image processing apparatus (Fig.2) comprising a memory device (114, 124, 126, 135); a first processing means (114, 125,

140) for converting a plurality of color data into a plurality of image color data in a first state (125), and the plurality of color data into a plurality of image color data in a second state (114 or 140); a second processing means (128-133, 142-144) to receive a plurality of the pixel data and to output data processed based on the input image data; a third processing means (136) to process image data output from the memory device (114, 124, 126, 127 or 135) and to output data processed based on the input image data; a first circuit to input the image data output from the memory device (114, 124) into the first processing unit (114, 125); a second circuit to input the image data output from the first processing unit (114, 125) into the memory device (126, 127) and also to input the image data output from the memory device (126, 127) into the second processing unit (128-133, 143, 144); a switch device (112, 113, 134) for selectively switch the first and second circuits (col. 4, lines 1 – col. 5, line 52).

Concerning claims 21-26, Yoshida further teaches that the same image data is input into the memory device and the second processing unit in parallel when the first circuit is selected by the switching device (Fig.2), (claim 21); the same image data is input into the first processing unit and the second processing unit in parallel when the second circuit is selected by the switching device (Fig.2), (claim 22); the second processing unit (144) determines an attribute of an image region based on image data of a pixel to be processed and pixels on the periphery of the pixel to be processed, and outputs data indicating the attribute (col. 5, lines 38-45), (claim 23); the first processing unit converts the input image data into image data of a different color system (scanner 32) to output the converted image data, (claim 24); the third processing unit (136) processes the image data output from the first processing unit to correct sharpness of an image (col. 5,

lines 47-50), (claim 25); the third processing unit (136) substantially simultaneously receives the image data from the first processing unit (114, 125, 140) and data corresponding to the image data from the second processing unit (144, 142, 131, 132, 133), (claim 26).

Concerning claim 27, Yoshida discloses an image processing apparatus (Fig.2) comprising a memory device (114, 126, 127, 135); a first processing means (114, 125, 140) for sequentially convert and output the image data; a second processing means (128-133, 142-144) for receive the same image data (Cb, Cr, V) as input into the memory device and to output data processed based on the received image data; a third processing means (136) to receive the image data output from the first processing unit and the data output from the second processing unit, and to process the image data output from the first processing unit based on the data output from the second processing unit; an image forming unit (printer) to form an image on a sheet based on image data output from the third processing unit (col. 4, lines 1 – col. 5, line 52).

Concerning claim 28, Yoshida discloses an image processing apparatus (Fig.2) comprising a memory device (114, 124, 126, 135); a first processing means (114, 125, 140) for converting a plurality of color data into a plurality of image color data in a first state (125), and the plurality of color data into a plurality of image color data in a second state (114 or 140); a second processing means (128-133, 142-144) to receive a plurality of the pixel data and to output data processed based on the input image data; a third processing means (136) to process image data output from the memory device (114, 124, 126, 127 or 135) and to output data processed based on the input image data; a first circuit to input the image data output from the memory device (114, 124) into the first

processing unit (114, 125); a second circuit to input the image data output from the first processing unit (114, 125) into the memory device (126, 127) and also to input the image data output from the memory device (126, 127) into the second processing unit (128-133, 143, 144); a switch device (112, 113, 134) for selectively switch the first and second circuits; an image forming unit (printer) to form an image on a sheet based on image data output from the third processing unit (col. 4, lines 1 – col. 5, line 52).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Madeleine AV Nguyen whose telephone number is 571 272-7466. The examiner can normally be reached on Monday, Tuesday, Thursday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A. Williams can be reached on 571 272-7471. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Madeleine AV Nguyen
Primary Examiner
Art Unit 2626

September 6, 2005